WHAT IS CLAIMED IS:

1. An array of comparators, comprising:

a first, a second, and a third comparator;

an Exclusive OR gate having a first input connected to an output of said first comparator and a second input connected to an output of said second comparator; and

a variable current source connected to an output of said Exclusive OR gate, said variable current source supplying a bias current to said third comparator.

2. The array of comparators of claim 1, wherein said output of said Exclusive OR gate produces a signal that controls said variable current source.

3. The array of comparators of claim 2, wherein said bias current is increased by said variable current source according to said signal.

4. The array of comparators of claim 1, wherein said third comparator is arranged in the array of comparators between said first comparator and said second comparator.

5. The array of comparators of claim 1, wherein said third comparator comprises a latch circuit configured to receive said bias current.

6. The array of comparators of claim 5, wherein said latch circuit comprises a cross connected pair of transistors connected between a reset switch and a supply voltage, and having a first port capable of receiving a first current signal and producing a first output voltage, and a second port capable of receiving a second current signal and producing a second output voltage.

7. The array of comparators of claim 6, wherein said cross connected pair of transistors comprises:

a first MOSFET; and

a second MOSFET connected to said first MOSFET;

wherein:

a gate terminal of said first MOSFET is connected to a drain terminal of said second MOSFET;

a gate terminal of said second MOSFET is connected to a drain terminal of said first MOSFET; and

source terminals of said first and said second MOSFETs are connected to said supply voltage.

8. The array of comparators of claim 6, wherein said reset switch comprises a MOSFET connected between said first port and said second port.

9. The array of comparators of claim 1, further comprising:

a second Exclusive OR gate having an input connected to an output of said third comparator; and

a second variable current source connected to an output of said second Exclusive OR gate, said second variable current source supplying a second bias current to said second comparator.

10. An analog to digital converter, comprising:

an array of comparators, having respective inputs configured to receive an analog signal, and respective outputs configured to produce quantized signals responsive to said analog signal;

a priority encoder connected to said array of comparators, configured to produce a digital signal at an output responsive to said quantized signals;

an array of Exclusive OR gates, wherein each Exclusive OR gate of said array of Exclusive OR gates is configured to receive two of said quantized signals; and

an array of variable current sources, wherein each variable current source of said array of variable current sources is configured to provide a bias current to a corresponding comparator of said array of comparators, and is controlled by an output of a corresponding Exclusive OR gate of said array of Exclusive OR gates.

11. The analog to digital converter of claim 10, wherein said each Exclusive OR gate of said array of Exclusive OR gates produces a logic signal that controls a corresponding variable current source of said array of variable current sources.

12. The analog to digital converter of claim 10, wherein each comparator of said array of comparators includes a latch circuit configured to receive a corresponding bias current.

13. The analog to digital converter of claim 12, wherein said corresponding bias current is capable of being increased by a corresponding variable current source of said array of variable current sources.

14. In an array of comparators, a method for increasing a rate at which a comparator in a metastable condition transitions to a steady state, comprising the steps of:

(1) identifying, in the array of comparators, the comparator in the metastable condition; and

(2) providing a bias current to said identified comparator in the metastable condition, such that the rate at which the comparator in the metastable condition transitions to the steady state is increased.

15. The method of claim 14, wherein said providing step comprises the step of:

controlling a current output from a variable current source that provides the bias current for a latch circuit of said identified comparator in the metastable condition.

16. The method of claim 14, wherein said identifying step comprises the steps of:

(a) comparing a characteristic of a first comparator of the array of comparators with a characteristic of a second comparator of the array of comparators, wherein the first comparator and the second comparator are separated in the array of comparators by a third comparator in the array of comparators; and

(b) determining if the third comparator is the comparator in the metastable condition based on said compared characteristics.

17. The method of claim 16, wherein said comparing step comprises the step of:

receiving the characteristics as inputs to an Exclusive OR gate.

18. The method of claim 17, said providing step comprises the step of:

controlling a current output from a variable current source that provides the bias current for a latch circuit of said identified comparator in the metastable condition with an output of the Exclusive OR gate.

19. The method of claim 17, wherein said providing step comprises the step of:

connecting a first current source in parallel with a second current source to increase the bias current for a latch circuit of said identified comparator in the metastable condition.

20. The method of claim 19, further comprising the step of:

controlling a switch that connects the first current source in parallel with the second current source with an output of the Exclusive OR gate.

21. In an array of comparators that includes a first, a second, and a third comparator, a method for increasing a rate at which the third comparator transitions to a steady state, comprising the steps of:

(1) comparing an output of the first comparator with an output of the second comparator; and

(2) providing a bias current to the third comparator based on said compared first and second outputs.

22. The method of claim 21, wherein said comparing step comprises the step of:

receiving the first and second outputs as inputs to an Exclusive OR gate.

23 The method of claim 22, wherein said providing step comprises the step of:

controlling a variable current source that provides the bias current for a latch circuit of the third comparator based on an output of the Exclusive OR gate.

24. The method of claim 21, wherein said providing step comprises the step of:

connecting a first current source in parallel with a second current source to increase the bias current for a latch circuit of the third comparator.

25. The method of claim 25, further comprising the step of:

controlling a switch that connects the first current source in parallel with the second current source based on an output of an Exclusive OR gate.